## REMARKS

By this amendment, independent claims 1, 3, 5, and 7 are amended and claim 13 is canceled to place this application in condition for allowance. Currently, claims 1-12, and 14 are before the Examiner for consideration on their merits.

Claim 13 has been canceled since it is redundant in light of the limitations found in claim 5.

This response makes two points. The first is that the claims as now presented are supported by the specification, and the presence of the new claim limitation, the comparative showing in the specification, and the newly submitted article to Ryuta overcomes the rejection based on Tamatsuka.

The second point is that the article to Matsushita shows that an annealed structure akin to Tamatsuka does not produce a wafer with reduced COP levels below the surface, and such a structure is not the same as that claimed which, by the Examples of the specification, is such that the COP levels are low even in the face of repeated cleanings. More detailed arguments are presented below on each of these points.

This Amendment and RCE filing is also being made after numerous telephone discussions with the Examiner concerning the outstanding rejection.

To recap, the Examiner has cited the Tamatsuka reference to allege that this patent teaches a wafer having the same surface density of particles. It is also believed that there is no dispute that Tamatsuka teaches an annealing procedure to obtain a certain level of surface density of particles, and this contrasts with Applicants'

employment of a completely different process to obtain a wafer with the claimed level of surface density of particles.

That is, Applicants exercise control over the single crystal growing process in terms of time held at temperatures. This can be found in the specification on at least page 6 of the application. The criticality of the control is also shown in the comparative demonstration with the results shown in Figure 3 and Table 1. Therein, it is demonstrated that when the time and temperature control parameters are met, a surface particle density is obtained that is vastly improved over wafers that are not subject to this control.

To emphasize the unexpected performance of the wafers subjected to the control mentioned above, submitted herewith is an article entitled "Crystal-Originated Singularities on Si Wafer Surface after SC 1 Cleaning", and authored by Ryuta et al. (Ryuta). The gist of this article is the discovery that a new type of singularity or COP on silicon wafer surfaces has been discovered, and these singularities are formed as a result of SC 1 cleaning. The COPs are believed to originate from defects in the melt grown silicon crystals, see the last paragraph of Ryuta. The Examiner's attention is directed to Figure 3 of Ryuta. This figure clearly shows that the number of particles increases with repeated cleanings, and it is this problem that the present invention seeks to solve.

As evidenced by the comparative showing in the specification, Applicants have solved this problem by the aforementioned control, and this solution is deserving of patent protection. The results shown in the specification are totally unexpected in light of the teachings of Tamatsuka. As previously argued, there is no suggestion

whatsoever in Tamatsuka that a sliced or sliced and cleaned wafer could be produced with the claimed levels of particle density by control of the growing process.

Another issue raised by the Examiner is whether support exists for the proposed amendment that the surface density occurs in a wafer in a non-annealed condition. In this regard, the Examiner's attention is directed to lines 4-6 of the Abstract, page 4, lines 18-22, page 10, the last two lines, and page 12, lines 16-20. In each of these sections, the inventive wafer is described in terms of a grown single crystal silicon wafer that is sliced after growing.

In order for Applicant to be able to add the proposed limitation to the independent claims, the description must clearly allow persons of ordinary skill in the art to recognize that the Applicants invented what is claimed." **In re Gosteli**, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). Put another way, "the applicant must . . . convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention." **Vas-Cath v. Mahurkar**, 19 USPQ2d 1111, 1117, (Fed. Cir. 1991). How close the original description must come to comply with the description requirement of section 112 must be determined on a case-by-case basis. **Eiselstein v. Frank**, 34 USPQ2d 1467, 1470 (Fed. Cir. 1995).

It is respectfully submitted that one of skill in the art when reading the specification would readily understand that the inventive wafer in question, one that is already defined as having a sliced or sliced and cleaned surface is not an annealed wafer. There is no mention of annealing nor does annealing have anything to do with the advancement discovered by the inventors. Therefore, it is respectfully submitted that when applying the tests outlined above, the only reasonable conclusion is that the

claimed wafer can be defined having the particle density present in a non-annealed condition.

The Examiner should also realize that the present claim limitation does not say that the wafer cannot be annealed. It is only stating that the particle density value set forth in the claims exists in a non-annealed condition, and this is totally consistent with the original disclosure. Again, the claims do not state that no annealing takes place, just that the measured density occurs after slicing or slicing and cleaning, and without any annealing.

Having made the argument that the amendment to the claims is supported by the original disclosure, Applicants now contend that such claims are patentably distinguishable from the annealed wafer of Tamatsuka. As previously argued, the comparative evidence of the specification demonstrates that only through particular control of temperature and time can one obtain the claimed density levels of the non-annealed wafer. What this means is that the Examiner cannot contend that the pre-annealed wafer of Tamatsuka can contain the claimed surface density of particles because Tamatsuka does not teach the specific control of temperature and time during the single crystal growing process as is used to produce the claimed wafer.

Lacking a basis to conclude that Tamatsuka anticipates the claimed wafer, the Examiner is only left with somehow alleging that the claimed wafer is obvious in light of the teachings of Tamatsuka. However, there is no factual support for such a position. To make such an assertion without support is hindsight.

Even if such a position were put forth, the evidence in the specification demonstrates the criticality of the control of temperature and time during the growing

process, and this would effectively rebut any allegation made by the Examiner in this regard.

To summarize, the revisions to the independent claims preclude the Examiner from relying on Tamatsuka under 35 U.S.C. § 102(b). Moreover, there is no basis to make an obviousness rejection, and even if one were proffered, it would be rebutted by the showing set forth in the specification.

To further substantiate the patentability of the claims at hand, submitted herewith is another article take from Vol. 1 of the Proceeding of the Eighth International Symposium on Silicon Materials Science and Technology, entitled "Hydrogen Anneal of Silicon Wafer Formation of High Quality Device Active Layer" by Matsushita et al. (Matsushita).

The Examiner's attention is particularly directed to Figure 13 and page 686, lines 13-17. What this Figure shows is two things. First, the hydrogen annealed wafer (HI) is superior to a CZ wafer in terms of COP density. That is, the COP density for HI is significantly lowered as compared to the COP density of the CZ wafer. This is believed to be consistent with the teachings of Tamatsuka, wherein the annealing process is employed to improve wafer quality.

As importantly though, Figure 13 also shows that the HI process is still not effective in removing COP that are spaced from the surface of the wafer. For example, while HI 1, which is designated by the symbol □, shows virtually no COPs at the surface, significant numbers remain at depths of less than 2 microns.

This article is consistent with Applicants' previous arguments that the structure of the annealed wafer of Tamatsuka is not the same as that is claimed. What Figure 13

shows is that the COP density, while low at the surface of an annealed wafer, increases greatly, and repeated cleanings would result in a increased number of particles on the cleaned surface. Matsushita confirms independently that an annealed wafer such as Tamatsuka's does not have the same structure as a CZ wafer or a CZ wafer that is subjected to Applicants' process. If one were to speculate as to how the Applicants' wafer would look in Figure 13 of Matsushita, it would be a flat line at low COP density, the flatness indicating that the COP density in the body of the wafer is low throughout, such that the measured particle density after repeated cleanings remains low.

The stance that the wafer of Tamatsuka is not the same as that claimed is independent of whether the amendment regarding the non-annealed condition is present or not. Referring again to the Ryuta article, page L1949, col. 1, the paragraph beginning on line 5, the SC 1 cleaning results in removal of a very thin surface layer. Therefore, the annealed wafer of Matsushita and Tamatsuka would exhibit increased surface particle density after repeated cleanings. This phenomenon does not occur with the claimed wafer as is shown in Table 1 and Figure 3 of the specification. Therein, the wafers processed according to the invention show a particle density of less than 15 counts/cm$^2$ after 6 cleanings. Example 1 and Figure 3 show that counts/cm$^2$ are less than 1 after three cleanings. To reiterate, it is submitted that even if the Examiner were to reject the claims under 35 U.S.C. § 112, first paragraph, as containing new matter, the claims without this objectionable limitation are still patentably distinct over Tamatsuka on the grounds that the annealed wafer of this patent is not the same as the sliced and or sliced and cleaned wafer of the invention.

Serial No.: 10/601,576

To summarize, Applicants contend that the rejection based on Tamatsuka should be withdrawn in the face of the amendments to claims 1, 3, 5, and 7, the article to Ryuta, and the showing in the specification, or be withdrawn even without the amendments to the claims in the face of the Matsushita article and its teachings that an annealed wafer has a different structure than the claimed sliced or sliced and cleaned wafer of the claims.

Accordingly, the Examiner is respectfully requested to examine this application in light of this amendment, and promptly pass claims 1-12, and 14 onto issuance.

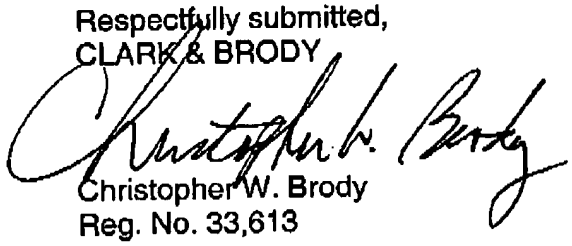
If the Examiner believes that a further interview with Applicants' attorney would help expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 202-835-1753.

The above constitutes a complete response to all issues raised in the outstanding Office Action of March 15, 2005.

Again, reconsideration and allowance of this application is respectfully requested.

Please charge any fee deficiency or credit any overpayment to Deposit Account No. 50-1088.

Respectfully submitted,
CLARK & BRODY



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# Crystal-Originated Singularities on Si Wafer Surface after SC1 Cleaning

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It is clarified that a new type of singularity is formed on Si wafer surface by the Standard Cleaning 1 (SC1) of the RCA cleaning process. Such singularities are perceived by laser particle counters as small particles on wafers. It is shown that the singularities correspond to small shallow pits caused by the etching effect of the SC1 cleaning solution. The origin of the pits is presumed to be some kind of defect in the melt-grown crystals.

KEYWORDS: silicon, cleaning, particle, defect

Since the particles on Si wafers degrade the LSI performance, many efforts have been made to reduce the number of particles. The minimum size of the particles to be eliminated has been related to the linewidth of the LSI devices. Particles larger than 0.1 μm may degrade the yield of half-micron devices. It has been supposed that the particles counted by widely used laser particle counters are dust on the wafers. Therefore, the cleaning process of wafers has been studied mainly to find ways to remove the particles. The SC1 cleaning,[1] cleaning by $NH_4OH/H_2O_2/H_2O$ solution, is known to be effective in reducing of the amount of dust. In this paper, it is clarified for the first time that most of the small particles are not dust on the wafers but pits formed during the SC1 cleaning.* It is suggested that such pits originate from some defect in the Si crystals.

Polished (100) Si wafers, 6 inches in diameter and P-type, 10 Ω·cm were used in the present experiments. The wafers were cut from Czochralski (CZ) crystals with the oxygen level of $1.0\times10^{18}$ atoms/cm$^3$** unless otherwise noted. After SC1 cleaning and rinsing by deionized water, the particles were counted by a laser particle counter, Topcon WM3. The composition of the SC1 cleaning solution used in this study was $NH_4OH:H_2O_2:H_2O=1:1:5$, and the cleaning temperature and time were 90°C and 20 min respectively. In Fig. 1, the average number of the particles for a batch (25 wafers) of SC1 cleaning is shown. Wafers were cleaned repeatedly and the average number of the particles was plotted against the number of cleaning cycles. Here, the number of the particles is shown for each range of particle size: small size S(0.20–0.25 μm), medium size M(0.25–0.30 μm) and large size L(larger than 0.30 μm). It is important to note that the number of particles increases with the number of cleaning cycles. The number of the small-size particles increases from the initial stage of the repeated cleaning, whereas the numbers of the medium- and large-size particles increase afterwards.

$NH_4OH$ in the SC1 cleaning solution etches off the surface of Si wafer and may increase the roughness of the surface. Therefore such an increase in the number of the particles may be caused by the increase in the micro roughness of the wafer surface after SC1 cleaning. However, evaluation of the microroughness with a three-dimensional noncontact surface profiler, WYKO TOPO-3D, showed that the average microroughness of wafers after 10 times cleaning, 0.5 nm, was identical to that after first cleaning. Therefore the increase in the particle number with the number of cleaning cycles is not due to the increase in the microroughness.

Mechanical damage due to the lapping process of the wafers may remain even after the polishing process (20 μm off in this case) and may be the origin of the increase in the particle number. However, the duplicated

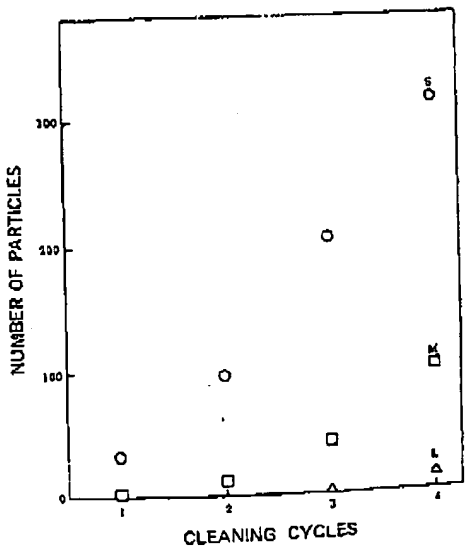



Fig. 1. Relationship between the number of particles and the number of cleaning cycles.

*In this paper, the term "particle" is used to signify the singularity detected by particle counters although it includes pits besides real particles (dust).

**The oxygen concentrations in this study were based on the conversion coefficient of IR measurement, $3.0\times10^{17}$ atoms/cm$^3$.[2]

polishing by 20 $\mu$m × 2 to remove the damage resulted in no change in the number of particles. Thus the lapping-induced damage is not the origin of the particles.

Figure 2 shows the result of repeated cleaning of epitaxial wafers (thickness of the epitaxial layer was 10 $\mu$m) by the same cleaning facility as used in Fig. 1. The open circles indicate the average numbers of small particles after repeated cleaning on 5 as-received epitaxial wafers; the filled circles indicate those on 5 epitaxial wafers polished off by 5 $\mu$m. It is clear that the number of particles on epitaxial wafers is not larger than 5 and does not increase with the number of cleaning cycles. These particles seem to be the dust on wafers after cleaning; the number of dust is almost constant for each cleaning process. Thus the increase in the particles number shown in Fig. 1 must be caused by something other than the dust. Figure 2 also clarifies that the mechanical damage due to the polishing process, if any, does not increase the number of the small-size particles.

Figure 3 shows the crystal dependence of the number of particles. The circles indicate the average numbers of small particles after repeated cleaning on 25 wafers of crystal A; the triangles indicate those on 25 wafers of crystal B. Crystals A and B were grown by using different growing systems. The rate of increase in the number of particles with the number of cleaning cycles differs greatly between the two crystals. It is plausible that the increase in the particle number with the number of cleaning cycles originates in some singularity in the melt-grown crystal. Measurements of the particle numbers on 25 CZ wafers (oxygen concentrations: $0.9 \sim 1.1 \times 10^{18}$ atoms/cm$^3$) and 25 magnetic field-applied Czochralski (MCZ) wafers (oxygen concentration: $0.6 \times 10^{18}$ atoms/cm$^3$) led to the conclusion that the particle number does not depend on the oxygen concentration if a similar growing system is used.

Next, the particle distributions on 25 wafers after repeated cleaning were inspected in detail. As a result, 36% of the small particles on wafers after the first cleaning remained as small particles in the same position after the second cleaning. On the other hand, 12% changed into medium-size particles and 52% disappeared during the second cleaning. Since the reproducibility of the particle position by the laser particle counter is not very accurate, the majority of small particles seem to remain as particles after the subsequent cleaning process; some remain as small particles and other particles change size to the medium range. Figure 4 shows an example. A small particle indicated by an arrow changed into the medium size after the 4th cleaning and further changed into the large size after the 7th cleanfing. Observations of such enlarged particles after 16 cleaning cycles were performed using a stereo-SEM. An example is shown in Fig. 5. A

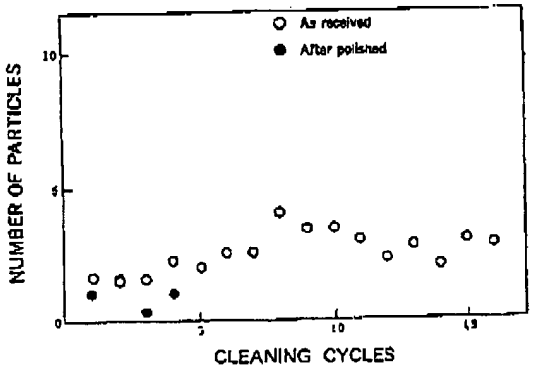



Fig. 2. Relationship between the number of small particles on epitaxial wafers and the number of cleaning cycles.

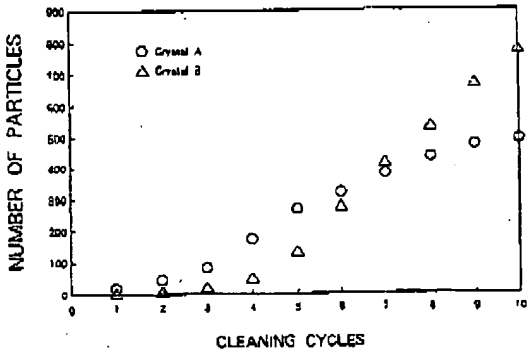



Fig. 3. The crystal dependence of the number of the particles.

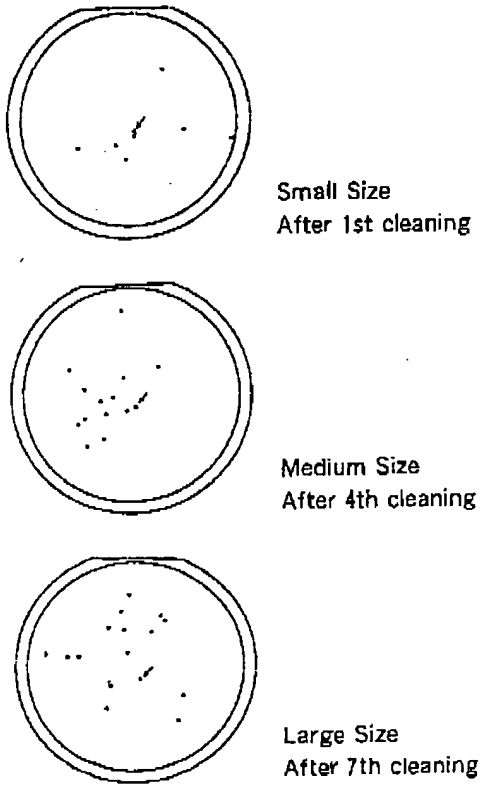
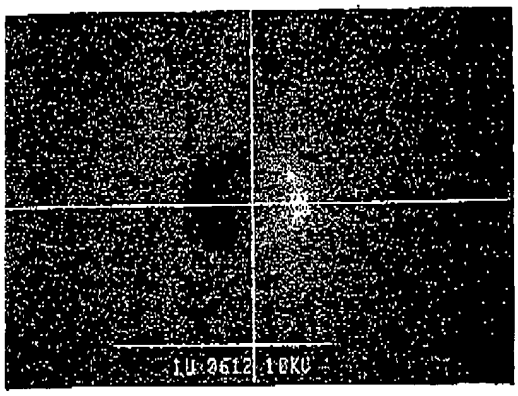
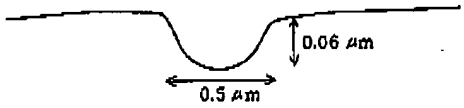



Fig. 4. The particle distribution on a wafer after repeated cleaning.




SEM image

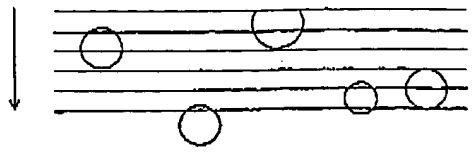



Sectional profile

Fig. 5. An observation of an enlarged particle by stereo SEM.

shallow pit 0.5 μm in diameter and 0.06 μm deep was found. Such small, shallow pits are rarely detected by normal SEM. Analyses of such pits by EPMA did not reveal the existence of metal impurity elements.

The important results obtained by this study are that the number of the particles increases with repeated SC1 cleaning and some of the particles change into the larger size range. This can be explained on the basis of a model shown in Fig. 6. By the etching effect of SC1 cleaning, a very thin surface layer is etched off by each cleaning process and the origins of pits within this surface layer make pits. If the origins of the pits exist randomly in the crystal, etching by the successive cleaning must make new pits. It is also assumed that the etching rate of SC1 cleaning is independent of the crystal orientation. If this is the case, the bottom and the side wall of a pit are etched at the same rate by successive cleaning process. Since the surface of the wafers is etched off at the same rate as the pits's inner surface, the depth of the pit does not change by the repeated cleaning, but the width of the pit enlarges. Thus, the laser particle counter detects increases in the number and size of the "particles."



The origins of the pits

The pits enlarged by repeated cleaning

Fig. 6. Schematic drawings of the origins of the pits and the pits enlarged by repeated cleaning.

The authors presume that the origin of the pits is some new type of defect in the melt-grown Si crystal. Pits are formed at such origins by SC1 cleaning and are detected by the laser particle counter as "particles". The authors named such "particles" crystal-originated "particles" (COPs). Investigations into the relationship between the crystal characteristics and COPs are in process.

In summary, a new type of singularity (COP) on Si wafer surfaces was discovered. Such singularities are formed by SC1 cleaning of Si wafers and detected by the laser particle counters as small-size particles on wafers. It has been shown that the singularities are due neither to the dust on wafers nor to the microroughness of the surface as a result of the etching during the cleaning process; the effects of the lapping and polishing process are also discounted. Detailed inspections confirmed that the singularities are indeed shallow pits on the wafer surface. The origins of COPs are presumed to be defects in the melt-grown Si crystals.

### Acknowledgement

The authors thank M. Kishimoto for his analyses of the particle data. They also thank Y. Wakisawa for his valuable discussions.

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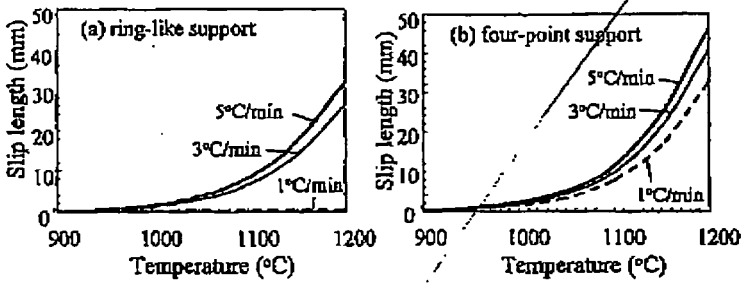


Fig.9. Calculated slip length during thermal processes as a function of annealing temperature at rates of 1°C/min ( -----), 3°C/min ( —— ) and 5°C/min ( ——): (a) ring-like support, (b) four-point support.

Table2. Maximum temperature to avoid slip.

(a) ring-like support

| ramping rate | slip length 1mm | 5mm | 10mm |
|---|---|---|---|
| 1°C/min | >1200°C | >1200°C | >1200°C |
| 3°C/min | 985°C | 1085°C | 1125°C |
| 5°C/min | 970°C | 1065°C | 1110°C |

(b) four-point support

| ramping rate | slip length 1mm | 5mm | 10mm |
|---|---|---|---|
| 1°C/min | 980°C | 1070°C | 1115°C |
| 3°C/min | 960°C | 1055°C | 1100°C |
| 5°C/min | 955°C | 1045°C | 1090°C |



# HYDROGEN ANNEAL OF SILICON WAFER FORMATION OF HIGH QUALITY DEVICE ACTIVE LAYER

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## ABSTRACT

The effect of hydrogen annealing is evaluated on the sub-surface quality in the silicon wafer. That has an advantageous effect both on the control of BMD (Bulk Micro Defect) and on the elimination of grown-in defects. The elimination of grown-in defect is observed not only at the surface but also in the sub-surface. The elimination is considered to be due to both oxygen under-saturation in the sub-surface and collaboration of vacancy diffusion and the surface atom migration in the defect during the hydrogen annealing.

The electrical properties, such as GOI (Gate Oxide Integrity) and so on, are improved by the hydrogen annealed wafer (Hi wafer). In addition, the quality of the Hi wafer using improved crystal is as high as that of an epitaxial wafer in the sub-surface. The Hi wafer is promising to a substrate of the sub-half micron devices.

## INTRODUCTION ; REQUIREMENT FOR SILICON WAFER

As a ULSI (Ultra Large Scale Integration) becomes the higher density and the finer pattern, characteristics of a substrate silicon wafer are the more effective on the ULSI performance. Especially, the quality of sub-surface of the silicon wafer, which is active region in the ULSI, dominates both production yield and reliability.

As well known, the silicon crystal grown in Czochralski (CZ) method has both supersaturated oxygen atoms(1) and grown-in defects(2). The supersaturated oxygen atoms induce the bulk micro defects (BMD's) due to oxygen precipitation during heat treatments. The BMD has high gettering efficiency for harmful impurities(3), then the BMD, induced in the interior far from the surface, is beneficial for ULSI. On the other hand, when the BMD's and/or the grown-in defects are introduced in the sub-surface, the fatal influence could be obtained on ULSI performance. Both the BMD and the grown-in defect must be taken out of the sub-surface. Therefore, the sub-surface quality of silicon wafer is one of the most important subjects. The ideal silicon wafer structure is considered as shown in Fig.1(4).

In order to improve the sub-surface quality, we have developed a hydrogen anneal of

silicon wafer(5,6), that is called Hi wafer. The sub-surface in the Hi wafer is improved to be defect free. And the BMD's are simultaneously induced in the interior far from the surface. The BMD depth distribution is controlled by using appropriate hydrogen anneal process.

In this paper, it is indicated that the effects of hydrogen anneal on improvement of both the sub-surface quality and the BMD distribution control. And we propose the as-grown defect elimination mechanism in the sub-surface, comparing to the annealing in other ambient.

## CONTROL OF BMD DENSITY

The BMD density is controlled by oxygen concentration in the silicon wafer, because that is induced by precipitation of supersaturated oxygen in silicon. Therefore if the oxygen concentration comes to lower than solid solubility limit (SSL) in silicon crystal, the oxygen can not precipitate, then the BMD can not be induced. As shown in Fig.2, oxygen concentration in sub-surface is lower than SSL after hydrogen anneal at 1200℃ for 1hr. In other ambient this cannot be achieved. Figure 3 shows the depth distribution of BMD density. The BMD density is clearly decreased toward the surface and it is achieved to be BMD free in sub-surface of Hi wafer. Moreover it has been observed that the BMD induced by pre-heating is eliminated in sub-surface during hydrogen anneal. This is because the precipitated oxygen atoms are resolved and diffused into silicon substrate.

The BMD density in interior can be also controlled by applying appropriate hydrogen anneal process. The hydrogen anneal is carried out at a temperature around 800℃ for putting into the furnace and ramping up to an annealing temperature as high as 1200℃. The putting temperature and ramp up rate are effective on BMD formation because BMD nucleation and growth occur at lower temperatures than 1000℃(7). The BMD density can be controlled by experience time during low temperatures, that is, the ramping up rate. Figure 4 shows the BMD density dependence on the oxygen concentration in the wafer after 2 step heat treatments of 780℃, 3hr. + 1000℃, 16hr, as a parameter of the ramping up rate. That in the case of CZ wafer is also shown as a reference. The BMD density is clearly decreased as the ramping up rate increased (indicated Hi(R) in Fig4). Then the BMD density is controllable by hydrogen anneal process.

## DETECTION OF GROWN-IN DEFECT

As well known, the silicon crystal has many grown-in defects(2,8). These grown-in defects are called as FPD (Flow Pattern Defect)(8), COP (Crystal Originated Particle)(9) or LSTD (Laser Scattering Tomography Defect)(10) depending on individual detection method. The FPD and COP are considered to be closely correlated each other or the same defect. The COP was recognized as a void by transmission electron microscopic observations(11). And some of inner surfaces in the voids are considered being covered



by thin oxide layer. Figure 7 shows an AFM (Atomic Force Microscope) image of the COP emerging on the surface after SC-1 ($NH_4OH$, $H_2O_2$, $H_2O$ solution) cleaning. Most of the COP's are observed as twin of a tetrahedral pit with the size about 100 to 300nm width and 100nm depth on the surface. The number of COP's are measured by a laser particle counter after SC-1 cleaning because it gives rise to laser scattering as well as a fine particle. The defect, giving rise to laser scattering, is called LPD (Light Point Defect). In order to define the COP correctly, it is necessary to distinguish between the COP's and the particles on the LPD map taken by the laser particle counter.

We use a following method to distinguish the COP. Applying a sequential cleaning by SC-1, the feature of COP becomes slightly wider. And the scattering center doses not change the position on the wafer. On the other hand, the particle would not keep the same position during the sequential cleanings. Then, comparing the position in the LPD map at each step of the sequential cleanings, we can distinguish between the COP and the particle. This method is called "a differential method". By using the differential method, it is possible to measure the COP number and size distribution on the full area of the wafer.

## EFFECT OF HYDROGEN ANNEAL ON GROWN-IN DEFECT ELIMINATION

Figure 8 shows the AFM images of the same position on the wafer before (a) and after (b) hydrogen anneal. The grown-in defect is observed as a twin pit, that is COP, on the CZ polished wafer surface before hydrogen anneal (Fig. 8 (a)). It is remarkable that the twin pit perfectly disappeared on the wafer surface after hydrogen anneal, that is, Hi wafer (Fig. 8 (b)). In other ambient such as oxygen and/or nitrogen, the COP survives after anneal, though the pit shape is slightly blunt as shown in Fig. 9.

Figure 10 shows the LPD density distribution of both CZ and Hi wafers. The measured LPD size is 0.14 micron or larger. The crystal ingot position used for the CZ and the Hi wafer was the same. Figure 10 includes the data of the wafers cut from several ingots. It is clear that the LPD density is drastically decreased in the Hi wafer. Therefore, the hydrogen anneal is very effective on the elimination of the surface COP.

For the ULSI performance, the sub-surface quality is very important because that comes to the device active region. Then we evaluate the COP distribution in depth direction. For the evaluation in depth direction, we apply two kinds of method. One (method 1) is the method measuring the COP after oxidation and removal. The other (method 2) is the method using re-polish. When the silicon wafer is oxidized, the oxidation front progresses into the wafer reflecting the trace of void feature as schematically shown in Fig. 11. The COP number, measured by the method 1, is the value integrated in the oxidized thickness, if the oxide is thin. When the oxide becomes thick, the COP pit shape near the original surface becomes blunt. And the pit comes to ambiguous shape not to be detected by the laser particle counter. The survival thickness of the COP was estimated about 400nm oxidation.

Figure 12 shows the COP depth distribution in the Hi wafer measured by the method 1. For the comparison, the COP distributions in a CZ wafer and an epitaxial wafer are shown

simultaneously. The defects in the epitaxial wafer would not be the same as COP but the other kind of defects such as hill-rock, micro mound and so on. In the Fig.12, HI-1, Hi-2 and Hi-3 indicate the Hi wafers produced by using conventional CZ crystals and S-Hi indicates the Hi wafer using a crystal improved to decrease the grown-in defect. The improvement to the grown-in defect was carried out by controlling the thermal history over 1080℃(12) during crystal growth. It is clear that the COP density is drastically decreased in the sub-surface of Hi wafer comparing to that in the CZ wafer. Therefore, the hydrogen anneal has strong effect on the elimination of the grown-in defect in the sub-surface. And near the surface region, the COP is perfectly eliminated. In the HI wafer using conventional CZ crystal, however, the COP density is increased in the region thicker than 500nm. This means that the elimination effect of the hydrogen anneal is not strong enough in the wafer deeper than 500nm.

Figure 13 shows the COP depth distribution to about 10 $\mu$m measured by the method 2. The COP density in the Hi wafer is clearly lower than that in the CZ wafer, though a half or a quarter of COP's are left in the deep region. This means that the hydrogen anneal is not only effective near the surface but also in the deep region on the COP elimination. But the effect in the deep region is not so perfect as that near the surface.

In the case of the wafer improved to decrease the grown-in defect density, the COP density after hydrogen anneal is as low as or lower than that in the epitaxial wafer even in the region deeper than 500nm, as shown in Fig. 12. Then, the Hi wafer using the COP improved crystal is considered to have the same quality as the epitaxial wafer at least in the device active region. This Hi wafer is named "Super HI wafer".

## ELIMINATION MECHANISM OF GROWN-IN DEFECT

The COP feature in depth direction was observed by AFM using the re-polished wafer samples. Figure 14 shows the COP features in the CZ and Hi wafers at each re-polishing stage. Both single pit type and twin pit type were observed. In the CZ wafer, the COP's having both types were observed at the every stage of re-polishing. On the other hand, in the Hi wafer, most of COP's have single pit type near the surface region and those have both types in the deep region as well as the case of CZ wafer. Ratio of twin pit type is shown in Fig.15 as a function of re-polished thickness.

From Fig. 12, Fig. 13 and Fig. 15, the elimination mechanism of the grown- in defect by hydrogen anneal is considered as follows. The grown-in defect has initially either twin type or single type void. The twin type void turns into single type and finally disappeared during the hydrogen anneal. This change would be due to vacancy diffusion into silicon matrix and to void inner surface reconstruction by surface atom migration. Because the high temperature treatment in hydrogen gives rise to surface migration as shown in Fig. 16. Figure 16 shows the surface morphology taken by AFM of the wafer before (a) and after (b) hydrogen annealing. The CZ wafer has a relatively rough surface with random spacing (Fig. 16 (a)). After hydrogen annealing, however, the wafer surface has a step structure as shown in Fig. 16 (b). The step height, which is defined as 0.14nm by AFM, is corresponding to single atomic layer on the (100) silicon surface. The surface step and



atomic arrangement are schematically shown in Fig. 17. And this surface shows 2x1 structure. Anyway, the surface was reconstructed during the hydrogen annealing. Presumably, the high temperature heat treatment has more responsible for the surface reconstruction than the ambient of the heat treatment. The surface atoms migrate and reconstruct the void surface. Simultaneously, the vacancies are diffused into silicon matrix. Then the void shrinks and finally disappears. Therefore, the grown-in defects are decreased in the deep region but not perfectly eliminated.

On the other hand, the grown-in defect is perfectly eliminated in the sub-surface by the hydrogen annealing. This effect is especially recognized in the hydrogen ambient. Some of the void inner surfaces are covered by oxide film as indicated before. The oxide film would prevent the surface atom migration. If the covered oxide is removed, the surface atoms can freely migrate and reconstruct the surface during high temperature heat treatment. In the case of hydrogen annealing, the oxygen concentration in the sub-surface is lower than the solid solubility limit in silicon crystal. Figure 18 shows the oxygen out-diffusion profile calculated near the surface in the case that initial the oxygen concentration in the bulk is $8.7\times10^{17}$ atoms/cm$^3$ (This value corresponds to $1.4\times10^{18}$ atoms/cm$^3$ in old ASTM). The solid solubility limit of oxygen is about $6\times10^{17}$ atoms/cm$^3$ at 1200℃(13). In the region shallower than 0.4 nm, the oxygen is under-saturated over one order. Therefore, oxygen atoms are easily soluble in the silicon matrix at the sub-surface. The oxide covering the void surface is decomposed by the reduction effect of hydrogen and oxygen is diffused into the silicon matrix. At last, the void surface comes to bare surface without the oxide film. Then, the surface atoms of the void are mobile to reconstruct and the vacancy is diffused into the silicon matrix. Finally, the grown-in defect is eliminated at the sub-surface.

The elimination would not perfectly occur by the annealing in other ambient such as oxygen, nitrogen and so on. Because the oxygen concentration does not decreased so low as that in the hydrogen ambient. And the covering oxide, that stabilizes the void surface, would not disappear.

## ELECTRICAL PROPERTIES OF HI WAFER

It is well known that the Hi wafer improves the GOI (Gate oxide integrity)[14]. The improvement is recognized in both TZDB (time zero dielectric break down) and TDDB (time dependent dielectric breakdown). In addition, the improvement is observed in the gate oxide with wide range of thickness (7nm to 70nm). The Hi wafer was firstly developed in order to improve the gate oxide quality in DRAM (Dynamic random access memory). Recently that is applied in the MOS devices with a fine design rule such as DRAM, flash memory, logic and so on. In those devices, the thickness of gate oxide comes to thinner and thinner in obedience to the design rule. Then the gate oxide quality becomes the more serious problem.

The Hi wafer is effective on the GOI improvement for both the initial surface and the surface after sacrificial oxidation. The improvement was recognized even in the Hi wafer after 800nm sacrificial oxidation(14). After re-polishing, however, the GOI improvement

is slightly worse than that in the initial Hi wafer as shown in Fig. 19. The GOI is considered to be influenced by both the BMD(15) and the COP(16). The BMD is free in the sub-surface to about 10 micron of the Hi wafer. Then the degradation should be due to the COP. Figure 20 shows the correlation between the COP density and the gate oxide defect density. The gate oxide thickness is 20 to 30 nm. It is clear that the gate oxide defect correlates to the COP with nearly one to one correspondences.

In order to improve the GOI degradation in the sub-surface, the improved crystal, which was developed by controlling thermal history and heat stability at the solid-liquid interface in the crystal growth, was used in hydrogen annealing. That is called super Hi wafer. Since the COP in the sub-surface of super Hi-wafer is as low as that of the epitaxial wafer, the GOI keeps high grade even in the wafer after re-polish.

## SELECTION OF THE SUITABLE WAFER FOR ULSI

It has been founded from the application of CZ wafer to the sub-half micron device that the grown-in defects have a serious influence on the device performance (17,18). So far, since the design rule of the device was large enough in comparison to the size of grown-in defects, it had not serious influence on the device performance. Recently, however, as the design rule gets to be comparable to the grown-in defect size, its effect cannot be negligible. The influence of the grown-in defect, such as the COP, is schematically summarized in Fig. 21.

In order to get rid of the grown-in defect from the device active region, recently, the epitaxial wafer has been widely studied. This is because the epitaxial wafer has not such a defect as void in the epitaxial layer. The grown-in defect has been also eliminated in the super Hi wafer sub-surface, which acts as the device active region. Therefore, the super Hi wafer is also applicable to the sub-half micron devices.

The epitaxial wafer has another superior property, which is high controllability of the resistivity in both the epitaxial layer and the substrate, independently. The epitaxial wafer with a heavily doped substrate, like a p/p+ epitaxial wafer, has a high ability for latch-up endurance. On the other hand, the latch-up endurance is difficult for the Hi wafer. This is one of the reasons why the epitaxial wafer is used in the sub-half micron devices. However, the latch-up is possible to be prevented by forming a buried layer with heavy dope(19). The buried layer is formed by high-energy ion implantation. The high-energy ion implantation would be usually used for the well formation in sub-half micron devices. Therefore, the super Hi wafer is promising to the sub-half micron devices.

## CONCLUSIONS

It is proved that the hydrogen annealing has a strong effect on the improvement of the sub-surface in CZ wafer. That is effective on both the BMD control and the grown-in defect elimination. The grown-in defect is perfectly eliminated in the wafer sub-surface by the hydrogen annealing. The elimination of the grown-in defect is deduced from both the oxygen under-saturated in sub-surface and the surface atom migration.



The Hi wafer has a strong effect on the improvement of GOI in the sub-surface of the wafer. It is found that the GOI is correlated with the COP density. Both the oxidation method and the re-polishing method are used for the evaluation of the COP under the sub-surface. It is found in the super Hi wafer, the COP is perfectly eliminated even in the region deeper than 500nm. The device active region of super Hi wafer has high quality as well as that of epitaxial wafer. It is declared that the super Hi wafer is promising to the substrate for the sub-half micron devices.

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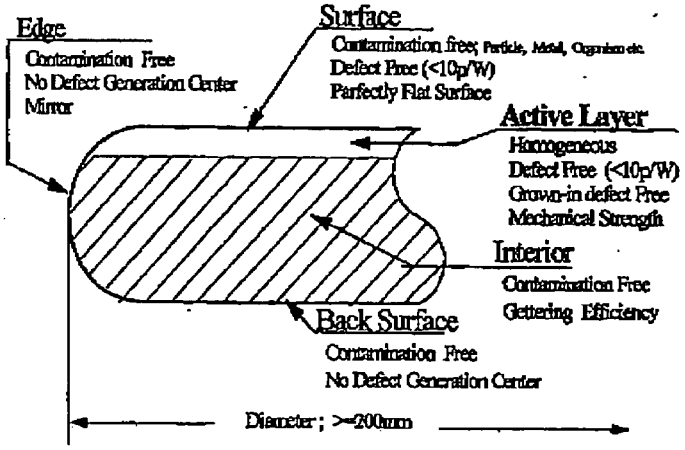



Fig.1. Silicon wafer structure required for ULS

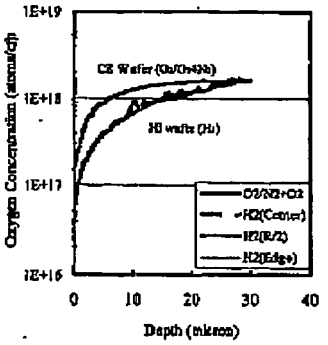



Fig.2. Oxygen depth profile measured by SIMS.

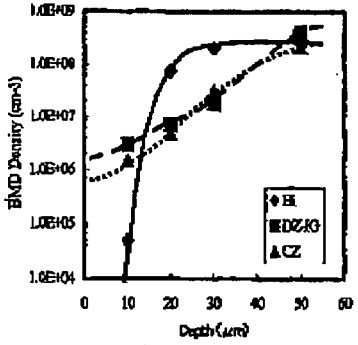



Fig. 3. Depth distribution of BMD density.



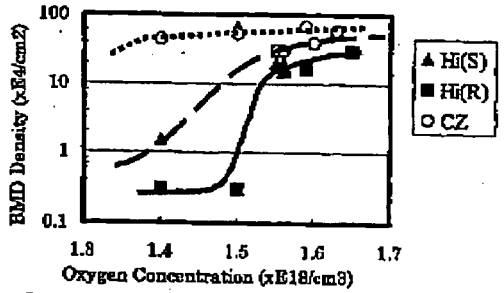



Fig. 4. BMD density as a function of initial oxygen concentration.

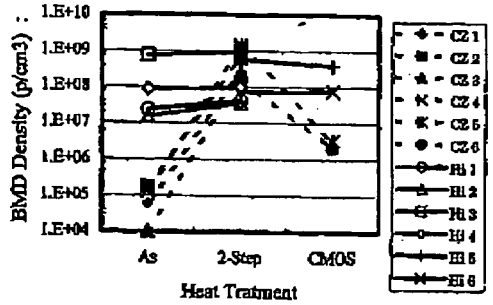



Fig.5. BMD density dependence on heat treatment proc ess.

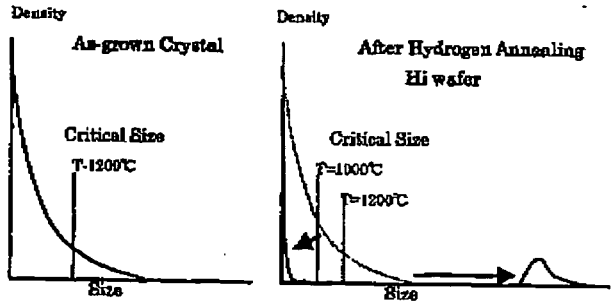



Fig.6 Schematic drawing of BMD nuclei distribution of Hi wafer.

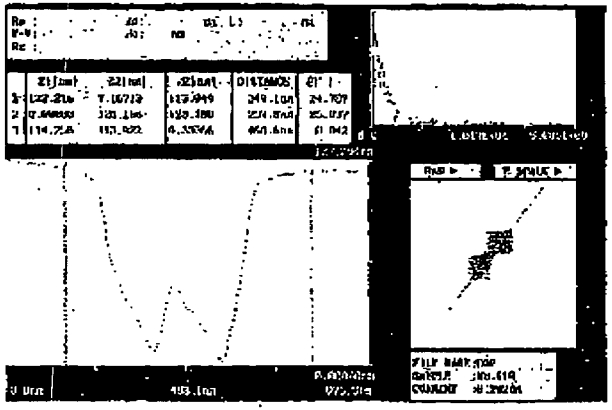
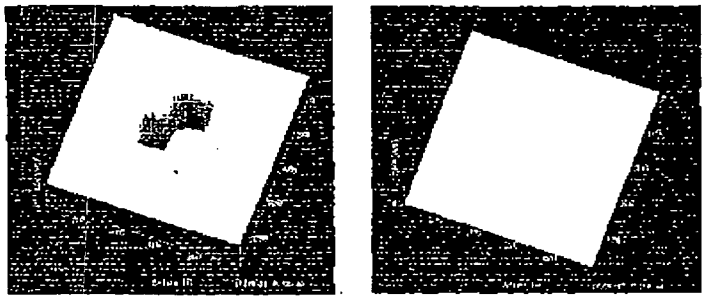


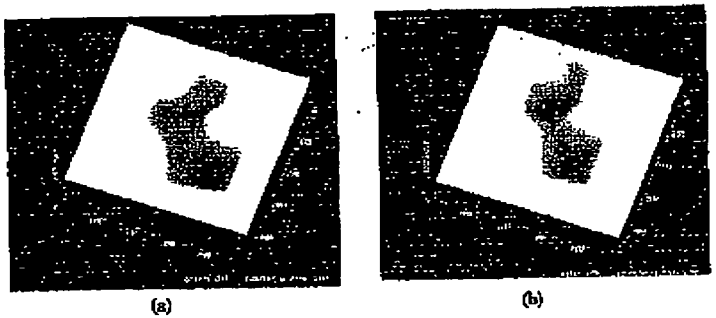
Fig. 7. AFM image of COP (Twin pit type)



(a) (b)

Fig. 8. AFM images at the same position before (a) and after (b) hydrogen anneal. The COP, observed before hydrogen anneal (a), perfectly disappeared by the hydrogen anneal.





(a) (b)

Fig. 9. AFM image of COP feature before (a) and after (b) oxidation.

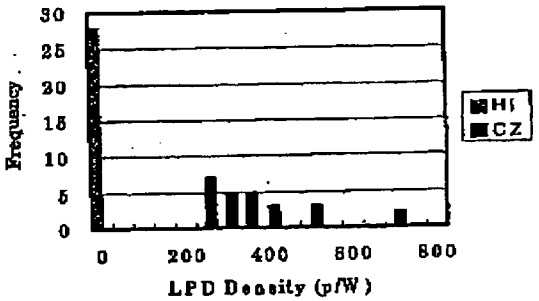



Fig. 10. LPD density distribution of CZ and Hi wafers.

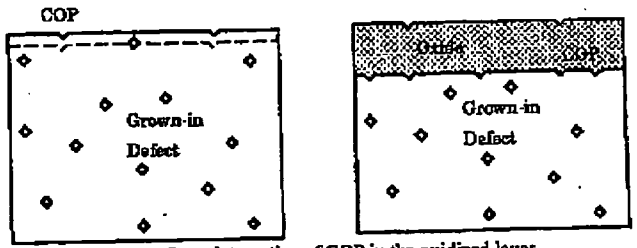



Fig. 11 Oxidation front reflects integration of COP in the oxidized layer.

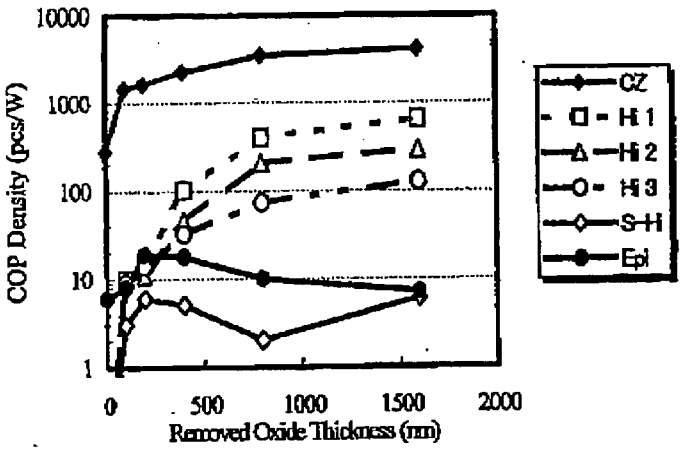



Fig. 12. COP distribution in-depth direction. The COP is measured by the oxidation and removal method.

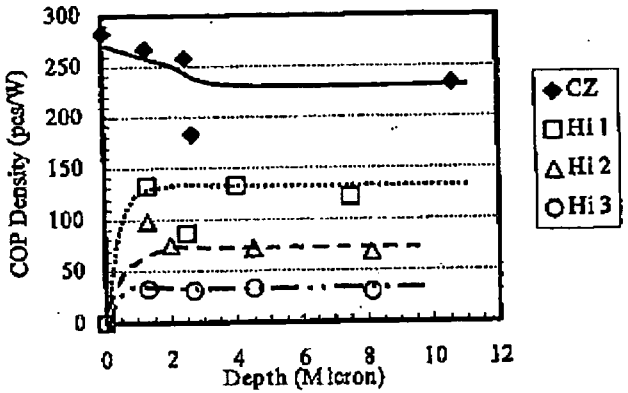



Fig. 13 COP distribution in-depth direction after re-polishing.



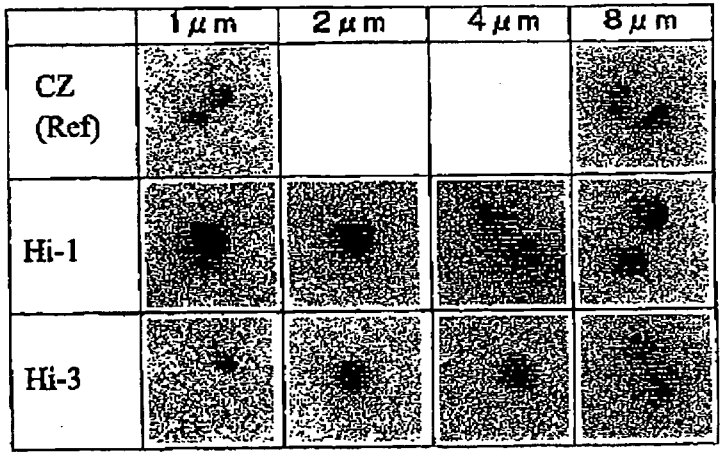



Fig. 14 AFM images of the COP revealed by re-polishing.

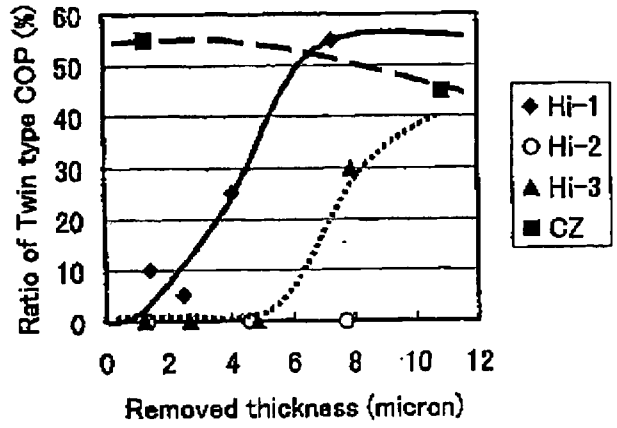



Fig. 15. Ratio of twin pit type as a function of re-polished thickness.

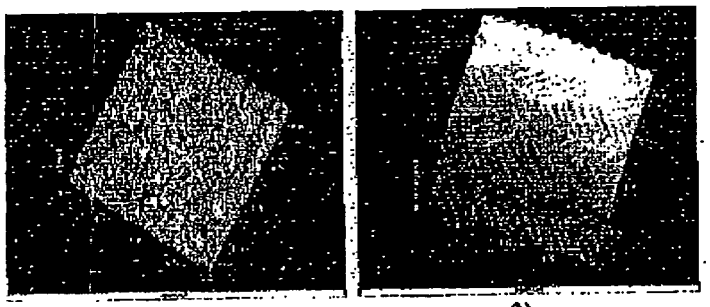



Fig.16. AFM image of the surface morphology. (a) Polished wafer, (b) Hi wafer.

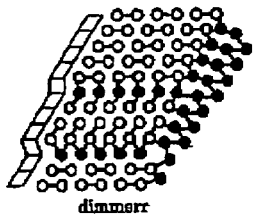



Fig.17. The step structure and atomic arrangement on the Hi wafer surface.

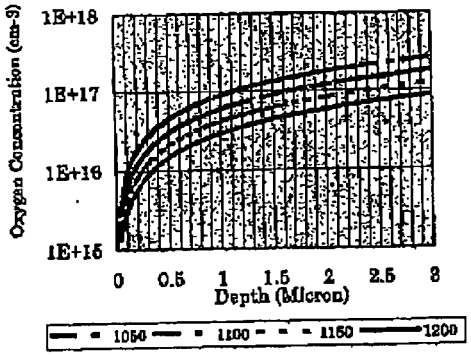



Fig.18. Oxygen out diffusion profile



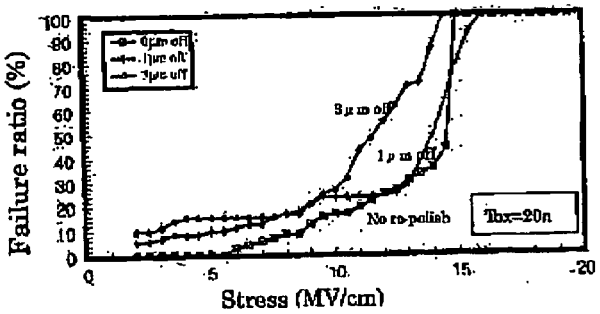



Fig.19 TZDB characteristics in re-polished Hi wafer.

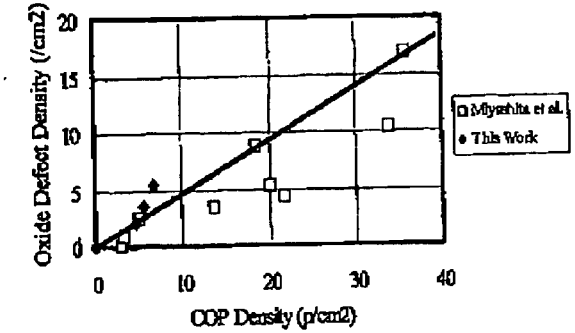



Fig. 20. Correlation between the oxide defect density and the COP density

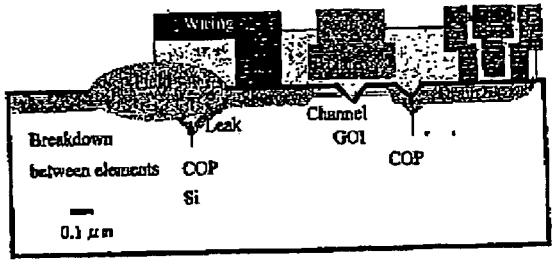



Fig. 21 Effect of COP on the device performance